ABSTRACT

A design verification system for developing electronic systems and methods for manufacturing and using same. The design verification system comprises a plurality of system elements, including at least one physical (or hardware) element and/or at least one virtual (or software) element, which are coupled, and configured to communicate, via a general communication system. Since the system elements may be provided on dissimilar development platforms, each system element is coupled with the communication system via a co-verification interface, which is provided as a layered protocol stack to assure portability and flexibility. Through use of the co-verification interface, the design verification system can be configured to support a wide variety of mixed physical/virtual systems.